REMARKS/ARGUMENTS

Claims 1-15 are pending in this application.

Objection to the Declaration

The declaration is objected to for not identifying the filing of International Application PCT/US03/11627 on which priority is claimed. A supplemental Declaration including the identification of the filing of International Application PCT/US03/11627 is being obtained and will be provided upon receipt. Upon receipt and filing of this supplemental Declaration, it is respectfully submitted that this requirement will be satisfied.

Objection to the Drawings

Figure 1 has been objected to for omitting the legend "—Prior Art—". However, the drawings must be read in the light of specification. While Figure 1 of the subject application illustrates a block diagram of a receiver system similar in image to that of Figure 1 of Wang, the elements of the present claimed invention as depicted in the drawings perform distinct functions from the elements shown in Figure 1 of Wang. Thus, when the drawings are taken in context with the corresponding description in the specification, Figure 1 is not illustrating a prior art system and applicants respectfully submit it would not be proper to identify the Figure as such. In view of the above remarks regarding Figure 1 it is respectfully submitted that this objection is satisfied and should be withdrawn.

Rejection of Claims 1, 3-6, 8 and 10-14 under 35 USC § 102(b)

Claims 1, 3-6, 8 and 10-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Janesch et al (U.S. Patent No. 6,072,842).

The present claimed invention provides a method and apparatus for establishing timing synchronism between a transmitter symbol clock and a local symbol clock in a receiver for receiving a signal transmitted as a sequence of symbols at a symbol frequency and subject to exhibiting a symbol frequency offset. A preselected number of offset values for a desired symbol timing recovery range are calculated. The offset values are grouped substantially symmetrically about a central offset value. Each of the preselected offset values is tested to see if symbol timing recovery lock can be achieved starting at the central offset value and gradually moving away from the central offset value. Independent claims 1 and 8 include features similar to those discussed above and thus the arguments presented below apply to each of these claims.

Janesch neither discloses nor suggests "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as recited in the present claimed invention. Additionally, Janesch neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention.

Janesch describes a carrier-recovery loop for a receiver in a communication system with features that facilitate initialization of the loop. The carrier-recovery loop is a PLL that uses a feedback signal to keep a recovery oscillator phase-locked to the carrier of a received signal. An initializing value is generated to bring the recovered signal to an initial frequency that approximates the carrier frequency. This is unlike the present invention which recites calculation of **a preselected number of offset values for a desired symbol timing recovery range**. The offset values are grouped substantially symmetrically about a central offset value. Each of the preselected offset values is tested to see if symbol timing recovery lock can be achieved by starting at the central value and gradually moving away from the central value. Thus, the present invention assures quick and accurate locking of the receiver clock with the transmitter clock by using algorithms to calculate a preselected number of offset values to cover the anticipated entire range that the STR is likely to traverse. Janesch merely describes

generating **a single initializing value** for bringing the recovered signal to an initial frequency that approximates the carrier frequency. The single initializing value functions as a starting point for the carrier-recovery loop. Therefore, the number of signal values generated depends on how far the initializing value is away from the desired phase lock. Thus, Janesch neither discloses nor suggests "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset values being grouped substantially symmetrically about a central offset value" as recited in claim 1 of the present invention.

Furthermore, the office action contends that column 2, lines 36-43 of Janesch disclose calculating a preselected number of offset values for a desired symbol timing recovery range. Specifically, the office action asserts that a comparison between the received signal and the feedback signal is conducted and a difference is measured in the phase detector 164. The difference then adjusts the feedback signal by a predetermined number until the received signal and the feedback signal are equal. Contrary to the assertions of the Office Action, column 2, lines 36-43 describe an initializing value is chosen to bring the recovered signal to an initial frequency that approximates the carrier frequency. While the loop process measures a difference in phase detector and adjusts the feedback signal accordingly, the number of measured difference values is not preselected. The loop process continues to make adjustments until the received signal and the feedback signal are equal. In contrast, the present invention provides a preselected number of offset values for a desired symbol timing recovery range to lock the receiver clock with the transmitter clock quickly and accurately. Such feature is neither disclosed nor suggested by Janesch.

Additionally, since Janesch is not concerned with calculating a preselected number of offset values for a desired symbol timing recover range, Janesch also cannot disclose nor suggest "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of present claimed invention. Janesch describes an initializing value is chosen to bring the recovered signal to an initial frequency that approximates the carrier frequency. The

initializing value functions as a starting point for a loop process that measures a difference in phase detector and adjusts the feedback signal accordingly until the received signal and the feedback signal are equal. Therefore, Janesch is concerned with a loop process that starts the testing with an initial value and an undetermined number of adjustments. This is unlike the present claimed invention which provides a preselected number of offset values for testing to achieve a desired symbol timing recovery lock quickly and accurately. Thus, Janesch neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of present claimed invention.

In view of the above remarks regarding claims 1 and 8 it is respectfully submitted that Janesch does not anticipated the present invention as claimed in independent claims 1 and 8. As claims 3-6 and 10-14 are dependent on claims 1 and 8 respectively, it is respectfully submitted that these claims are also patentable for the same reasons as claims 1 and 8 discussed above. It is thus further respectfully submitted that this rejection is satisfied and should be withdrawn.

Rejection of Claims 2 and 9 Under 35 U.S.C 103(a)

Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Janesch et al (U.S. Patent No. 6,072,842) in view of Wang (U.S. Patent No. 6,266,380).

Wang, similar to Janesch, neither discloses nor suggests "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as in the present claimed invention. Additionally, Wang, similar to Janesch, neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention.

Wang describes a system for eliminating DC offset in a received HDTV signal. A receiver processes a VSB modulated signal containing terrestrial broadcast high definition television information. A pilot component includes an input analog-to-digital converter for producing a datastream which is oversampled at twice the received symbol rate. A segment sync detector uses an abbreviated correlation reference pattern to recover a twice symbol rate sampling clock for the digital converter. A DC offset associated with the pilot component is removed from the demodulated signal before it is applied to an NTSC interference detection network. However, similar to Janesch, Wang neither teaches nor discloses "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset values being grouped substantially symmetrically about a central offset value" as recited in the present claimed invention. Wang is concerned with attenuating DC component from a demodulated symbol datastream. This is unlike the present claimed invention which is concerned with establishing timing synchronism between a transmitter symbol clock and a local symbol clock in a receiver for receiving a signal transmitted as a sequence of symbols at a symbol frequency and subject to exhibiting a symbol frequency offset.

Additionally, since Wang is not concerned with calculating a preselected number of offset values for a desired symbol timing recover range, Wang also cannot disclose nor suggest "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of present claimed invention. Wang describes a system for processing a received VSB signal containing high definition television information includes a compensation network for processing an oversampled symbol datastream at the oversampling rate to remove a symbol DC offset component. Therefore, Wang is concerned with attenuating DC component from a demodulated symbol datastream. This is unlike the present claimed invention which provides a preselected number of offset values for testing to achieve a desired symbol timing recovery lock quickly and accurately. Thus, Wang neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and

gradually moving away from said central offset value" as recited in claim 1 of present claimed invention.

Applicants respectfully submit that there is no reason or motivation to combine Janesch with Wang. Janesch describes a carrier-recovery loop of a radio receiver with an initializing value that brings the recovered signal to an initial frequency that approximates the carrier frequency. Wang describes a system for eliminating DC offset from a demodulated symbol datastream. These references are responsive to different problems and thus it is respectfully submitted that the combination of these references to produce the present invention would not be obvious. Janesch involves providing a "carrier-recovery loop with a reduced acquisition time" (col. 2, lines 22-23). Wang, on the other hand, provides an improved method of "processing an oversampled symbol datastream at the oversampling rate to remove a symbol DC offset component" (col. 1, lines 38-40).

Even if there was a motivation to combine these two references, the combination of the system of Janesch with the system of Wang would not produce the present invention as claimed. Instead, the system resulting from the above combination would yield a system that provides a carrier-recovery loop with an initializing value that brings the recovered signal to an initial frequency that approximates the carrier frequency in a VSB modulated signal with ability to eliminating DC offset from the signal. This is wholly unlike the present claimed invention. Specifically, the present claimed invention recites "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset values being grouped substantially symmetrically about a central offset value". The combined system of Janesch and Wang neither discloses nor suggests such feature. Consequently, it is respectfully submitted that the present invention as claimed is patentable over the cited reference when taken alone or in combination.

In view of the above remarks to the claims 2 and 9, it is respectfully submitted that there is no 35 USC 112 enabling disclosure in Janesch or Wang, when taken alone or in combination, which would make the present claimed invention unpatentable.

Thus, it is further respectfully submitted that this rejection is satisfied and should be withdrawn.

Rejection of Claims 7 and 15 Under 35 U.S.C 103(a

Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Janesch et al (U.S. Patent No. 6,072,842) in view of Guillemain et al (U.S. Patent No. 6,175,600).

Guillemain, similar to Janesch, neither discloses nor suggests "calculating a preselected number of offset values for a desired symbol timing recovery range, said offset values being grouped substantially symmetrically about a central offset value" as in the present claimed invention. Additionally, Guillemain, similar to Janesch, neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in the present claimed invention.

Guillemain describes a system for detecting the presence of a carrier wave in a digital signal that is available at a given frequency. The system delivers at least two baseband samples of the digital signal at each symbol time. A timing estimator responding to the baseband samples to provide an error signal corresponding to a phase error between the clock frequency that is to be recovered and a local clock frequency. A detection signal is generated when a level representative of the variance of the error signal reaches a threshold value. However, similar to Janesch, Guillemain neither teaches nor discloses "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset values being grouped substantially symmetrically about a central offset value" as recited in the present invention. Guillemain is concerned with detecting the presence or the absence of a signal carrier wave that is present at a given clock frequency. This is unlike the present claimed invention which is concerned with establishing timing synchronism between a transmitter symbol clock and a local symbol clock in a receiver for receiving a signal

transmitted as a sequence of symbols at a symbol frequency and subject to exhibiting a symbol frequency offset.

Additionally, since Guillemain is not concerned with calculating a preselected number of offset values for a desired symbol timing recover range, Guillemain also cannot disclose nor suggest "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of present claimed invention. Guillemain describes a timing estimator responsive to the baseband samples for delivering an error signal corresponding to the phase error between the clock frequency that is to be recovered and a local frequency. A detector for generates a detection signal indicating that a carrier wave has been detected whenever a level representative of the variance of the error signal reaches a threshold value. Therefore, Guillemain is concerned with detecting the presence of a carrier wave in a digital signal that is available at a given frequency. This is unlike the present claimed invention which provides a preselected number of offset values for testing to achieve a desired symbol timing recovery lock quickly and accurately. Thus, Guillemain neither discloses nor suggests "testing each of said preselected offset values to see if symbol timing recovery lock can be achieved by starting at said central offset value and gradually moving away from said central offset value" as recited in claim 1 of present claimed invention.

Applicants respectfully submit that there is no reason or motivation to combine Janesch with Guillemain. Janesch describes a carrier-recovery loop of a radio receiver with an initializing value that brings the recovered signal to an initial frequency that approximates the carrier frequency. Guillemain describes a system detecting the presence of a carrier wave in a digital signal that is available at a given frequency. These references are responsive to different problems and thus it is respectfully submitted that the combination of these references to produce the present invention would not be obvious. Janesch involves providing a "carrier-recovery loop with a reduced acquisition time" (col. 2, lines 22-23). Guillemain, on the other hand, provides an improved method of detecting the presence of a signal carrier wave that combines

"speed, reliability, operation at a poor ED/No ratio (close to 2 dB), and is relatively insensitive to drift in the frequency of the carrier wave" (col. 2, lines 23-29).

Even if there was a motivation to combine these two references, the combination of the system of Janesch with the system of Guillemain would not produce the present invention as claimed. Instead, the system resulting from the above combination would yield a system that provides a carrier-recovery loop with an initializing value that brings the recovered signal to an initial frequency that approximates the carrier frequency with the function of detecting the presence or absence of a signal carrier wave. This is wholly unlike the present claimed invention. Specifically, the present claimed invention recites "**calculating a preselected number of offset values for a desired symbol timing recovery range**, said offset values being grouped substantially symmetrically about a central offset value". The combined system of Janesch and Guillemain neither discloses nor suggests such feature. Consequently, it is respectfully submitted that the present invention as claimed is patentable over the cited reference when taken alone or in combination.

In view of the above remarks to the claims 7 and 15, it is respectfully submitted that there is no 35 USC 112 enabling disclosure in Janesch and Guillemain, when taken alone or in combination, which would make the present claimed invention unpatentable. Thus, it is further respectfully submitted that this rejection is satisfied and should be withdrawn.

Having fully addressed the Examiner's rejections, it is believed that, in view of the preceding remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at the phone number below, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,
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